WE CLAIM:

1. A latching circuit that senses and latches the magnetic states of a first bit line and a second bit line in a magnetoresistive random access memory (MRAM), the latching circuit comprising:

a first output and a second output;

a reset circuit having a first terminal, a second terminal, and a third terminal, the reset circuit responsive to a first state of an input signal applied to the first terminal to couple the second terminal to the third terminal, and responsive to a second state of the input signal applied to the first terminal to decouple the second terminal from the third terminal;

a first switch having a first switching terminal, a second switching terminal and a control terminal, the first switching terminal of the first switch coupled to a first portion of the first bit line;

a second switch having a first switching terminal, a second switching terminal and a control terminal, the first switching terminal of the second switch coupled to a first portion of the second bit line;

a third switch having a first switching terminal, a second switching terminal and a control terminal, the first switching terminal of the third switch coupled to a second portion of the second bit line;

a fourth switch having a first switching terminal, a second switching terminal and a control terminal, wherein:

the first switching terminal of the fourth switch is coupled to a second portion of the first bit line;

the second switching terminal of the fourth switch is coupled to the second switching terminal of the second switch, to the control terminal of the first switch, to the control terminal of the third switch, to the second terminal of the reset circuit, and to the second output; and

the control terminal of the fourth switch is coupled to the control terminal of the second switch, to the third terminal of the reset circuit, to the

second switching terminal of the first switch, to the second switching terminal of the third switch, and to the first output.

2. A method of reading a magnetic state in a magnetoresistive random access memory (MRAM) cell, the method comprising:

selectively energizing a word line corresponding to the MRAM cell;

selectively energizing a first bit line that corresponds to the MRAM cell;

selectively energizing a second bit line that does not correspond to the MRAM cell;

temporarily resetting an interface circuit coupled to both the first bit line and to the second bit line such that an output of the interface circuit is reset to a balanced state;

comparing a voltage in a first portion of the first bit line to a voltage in a first portion of the second bit line;

comparing a voltage in a second portion of the first bit line to a voltage in a second portion of the second bit line; and

determining the magnetic state of the MRAM cell based at least partly on the comparisons of voltage.

3. The method as defined in Claim 2, further comprising generating an output with a logical state based at least partly on the determination of the magnetic state.

4. The method as defined in Claim 2, wherein selectively energizing the word line further comprises applying current to the word line.

5. A method of latching a magnetic state in a magnetoresistive random access memory (MRAM) cell, the method comprising:

selectively energizing a word line corresponding to the MRAM cell;

in a reset state, disabling cross-coupled feedback of an interface circuit coupled to a first bit line and to a second bit line, where disabling the cross-coupled feedback balances the interface circuit to current applied through first and second portions of the first bit line and through first and second portions of the second bit line, where the current applied to the first bit line and the current applied through the

second bit line are substantially equal, where the first bit line corresponds to the MRAM cell; and

in a latched state, enabling cross-coupled feedback across the interface circuit so that an imbalance in resistance from a stored state of the MRAM cell latches the interface circuit in a corresponding logical state.

6. The method as defined in Claim 5, wherein selectively energizing the word line further comprises applying current to the word line.